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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,297	12/31/2003	Jin-Hong Ahn	51876P540	9786

8791 7590 11/29/2005

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EXAMINER	
NGUYEN, DANG T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/749,297	AHN ET AL.
	Examiner	Art Unit
	Dang T. Nguyen	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,18-23 and 25-33* is/are rejected.

7)☒ Claim(s) *10-17 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This office action is in response to applicant's amendment filed on 9/22/05. Claims 1 – 2 and 4 – 33 are pending on this office action.

Claim Objections

2. In claim 27 there is no antecedent basis for the wording, "V_{wl}". There is not reference to " V_{wl} " earlier in the claim either in the form of an implied as well as a literal description from which an earlier antecedent reference may be made, there is no clear recitation in these claim to avoid possible confusion as to what is actually claimed. The claim fail to particularly point out and distinctly claimed the subject matter that the applicant considers to be the invention here. Clarification is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 9, 18 – 23, and 25 - 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamauchi, U.S. patent No. 6,009,011 – filed Dec. 24, 1997.

Regarding independent claim 1, Fig. 2 of Yamauchi discloses a method for operating a non-volatile dynamic random access memory (NVDRAM) device including a

plurality of memory cells (Fig. 5), each cell having a capacitor [C] and a transistor having a floating gate [FG], comprising:

preparing a power-on mode (Col. 9 lines 45 – 52; See Fig. 4 [Recalling/Initializing]) for performing a DRAM operation; and by controlling a threshold voltage of the transistor (Col. 9 lines 52 – 59); and

preparing a power-off mode (Fig. 4 [Is the power supply turned off ?]) for storing data (Fig. 4 [Storing operation]) included in the capacitor into the floating gate (Col. 9 lines 1 – 5).

Regarding dependent claim 2, Yamauchi discloses wherein the preparing the power (Fig. 4 [Recalling/Initializing]) on mode includes moving data stored in the floating gate into capacitor (Col.9 lines 45 – 52); and adjusting the threshold voltage of the transistor in all of the memory cells to a first threshold voltage (Table 3 lines 10 – 15).

Regarding dependent claim 4, Yamauchi discloses wherein the moving data includes charging capacitors of all memory cells with a logic high datum; (Col. 14 lines 58 – 64); and discharging the capacitor (Col. 11 lines 50 – 52 disclosing "transfer the charge from capacitor"), its floating gate storing a logic high datumn (Fig. 7 – 10).

Regarding dependent claim 5, Yamauchi discloses wherein the step moving data includes refreshing the plurality of capacitors (Col. 12 lines 50 – 50 – 54).

Regarding dependent claim 6, Yamauchi discloses wherein the plurality of the memory cells are arranged in a matrix by using a number of word lines and bit lines and the moving data (Fig. 4) is carried out in a row matrix (Fig. 17).

Regarding dependent claim 7, Yamauchi discloses wherein charging capacitors (Fig. 11- 16) includes supplying word lines connected to a multiplicity of the memory cells with a first threshold voltage in order to turn on the transistor in all the memory cells (Col. 13 lines 3 – 6); writing the logic high datum in the capacitors of the memory cell coupled to the word lines (Col. 14 lines 58 – 64); charging the capacitors and discharging capacitor (Fig. 4) in the memory having the transistor until all of the capacitors in the plurality of the memory cells are charged with the logic high datum (Fig. 11 – 16).

Regarding dependent claim 8, Yamauchi discloses wherein discharging the capacitor in the memory cell having the transistor (Fig. 11- 16) includes supplying all of the word lines with a second threshold voltage (Fig. 15a) in order to turn on the transistors, its floating gate storing the logic high datum; and supplying all the bit lines with about 0V (Fig. 15a) in order to discharge the capacitors in the memory cell having the transistor, its floating gate storing the logic high datum (data 1).

Regarding dependent claim 9, Yamauchi discloses wherein the adjusting the threshold voltage includes supplying all gates of the transistors in the all of the memory cells with a first predetermined voltage in order for fulfilling electrons in the floating gate (Col. 13 lines 54 – 57); charging all of the capacitors in all of the memory cells (Col. 14 lines 58 – 64); and decreasing the threshold voltage of the transistor to the first threshold voltage (Col. 14 lines 6 – 22).

Regarding dependent claim 18, Yamauchi discloses wherein the preparing the power-off includes removing electrons in the floating gate of the memory cell (Col. 9

lines 29-37) storing a logic High datum (Col. 9 line 55); discharging the capacitor by supplying gate of the transistors in all of the memory cells with a second threshold voltage (Fig. 7[12V]; See Col. 12 lines 5 – 29); repeating the step removing electrons in the floating gate (Col. 9 lines 29 – 37) of the memory cell storing the logic high datum until all the capacitors is discharged (Fig. 4).

Regarding dependent claim 19, Yamauchi discloses wherein the removing electrons includes: supplying a gate of the transistor in all of the memory cells with a negative voltage (TABLE 4 [-8V]) supplying a plate of the capacitor in the memory cells with a voltage level of a logic High datum (TABLE 4 [Vcc/2]).; selectively moving electrons in the floating gate to the capacitor storing the logic High datum (Col. 14 lines 58 – 64).

Regarding dependent claim 20, Yamauchi discloses wherein the discharging the capacitor by supplying gate of the transistor in al of the memory cells with a second threshold voltage (Fig. 7 [12V) includes supplying the gate of the transistor with a second threshold voltage (Fig. 7 [12V); and discharging the capacitor in some of the memory cells having the transistor turn on by the second threshold voltage (Fig. 7 – 10).

Regarding dependent claim 21, Yamauchi discloses wherein the discharging the capacitor includes refreshing the memory cell (Col. 12 lines 50 – 54).

Regarding claim 22, wherein the discharge capacitors is carried out row by row (Fig. 7 – 10).

Regarding dependent claim 23, Yamauchi discloses wherein the capacitor is a coupling capacitor (Fig. 2)

Regarding dependent claim 25, Yamauchi discloses wherein the moving data includes refreshing (Col. 50 – 54) the plurality memory cells by supplying each word line with a voltage level being higher than logic High datum (Table 2).

Regarding dependent claim 26, Yamauchi discloses wherein the moving data is carried out row by row (Fig. 11 – 16)

Regarding dependent claim 27, Yamauchi discloses wherein the supplying word lines further includes supplying other word lines wit a predetermined negative voltage except for the word line supplied with the Vwl (Fig. 8)

Regarding independent claim 28, Figs. 2 and 5 of Yamauchi disclose a non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells in a matrix (Fig. 5), each memory cell comprising:

A capacitor (Fig. [C]) for storing data; and

A transistor for transmitting the data stored in the capacitor (Fig. 2 [C]) to a bit line (Fig. 2 [BL]), wherein the transistor includes a drain, a source, and a gate having a control gate and a floating gate (Fig. 2 [FL]) for storing the data when power is off (Fig. 4 [Is the power supply turned off ?]) and a threshold voltage of the transistor (Table 3 an 4) is controlled when the power on (Col. 12 lines 55 - 62); wherein one terminal of capacitor (Fig. 2 [C]) is coupled to the drain of transistor and another terminal of the capacitor (Fig. 2 [C]) is supplied with a controllable voltage (Fig. 2 [CP]) determined according to an operation mode (Col. 11 lines 15 – 33).

Regarding dependent claim 29, Yamauchi discloses wherein the floating transistor is made of nitride (Col. 7 lines 5 – 7)

Regarding dependent claim 30, Fig, 2 of Yamauchi discloses wherein the gate of floating transistor [FG] formed in a single layer serves as a data storage (Col. 7 lines 9-12).

Regarding independent claim 31, Figs. 2 and 5 of Yamauchi disclose a nonvolatile dynamic random access memory comprises: a plurality of memory cells in a matrix (See Fig. 5), wherein each memory cell [MT] includes: a control gate layer (Fig.2, control gate coupled to WL) coupled to a word line [WL]; a capacitor (Fig. 2 [C]) for storing data; and a floating transistor (Fig. 2 [FG]) for transmitting the stored data in the capacitor (Fig. 2 [C]) to a bit line (Fig. 2 [BL]) and storing the data therein in response to an operation mode, wherein a threshold voltage of the floating transistor (Table 3 and 4) is controlled when the power is on (Col. 12 lines 55 - 62) wherein one terminal capacitor (Fig. 2 [C]) a drain of the floating transistor (Fig. 2 [FG]) and another terminal of the capacitor is supplied with a controllable voltage (Fig. 2 [CP]) determined according to the operation mode (Col. 11 lines 15 – 33).

Regarding dependent claims 32, Yamauchi discloses wherein the control gate layer is made of metal (Col. 7 lines 19-22) and the gate of floating transistor is made of nitride (Col. 7 lines 5 – 7).

Regarding dependent claim 33, Fig, 2 of Yamauchi discloses wherein the gate of floating transistor [FG] formed in a single layer serves as a data storage (Col. 7 lines 9-12).

Allowable Subject Matter

4. Claims 10 –17, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 10, in addition to other elements in the claim, the prior art does not teach or suggest "wherein the adjusting threshold voltage including backing up the captured data in the capacitor before the supplying all gates; and restored the backup data in the capacitor after the decreasing the threshold voltage".

With respect to claim 24, in addition to other elements in the claim, the prior art does not teach or suggest "wherein the voltage supplying a word line is defined by the following equations: $V_{wl} = V_{blp} + (V_{th-H} + V_{th-L})/2$".

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Prior art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nanba	Patent No. US 6,714,474 B2	Date of Patent: Mar. 30, 2004
Emori et al.	Patent No. US 6,314,017 B1	Date of Patent: Nov. 6, 2001

Contact Information

6. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 11/14/2005

VAN THU NGUYEN
PRIMARY EXAMINER